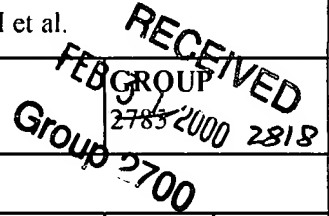
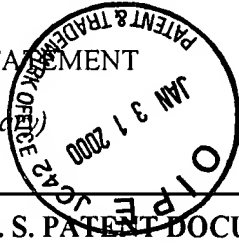


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INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>				APPLICANT ELIYAHOU HARARI et al.										
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TP	A1	4	0	9	0	2	5	8	5/16/78	Cricchi	365	184		
TP	A2	4	1	4	9	2	7	0	4/10/79	Cricchi et al.	365	222		
TP	A3	4	1	8	1	9	8	0	1/1/80	McCoy	365	185.03		
TP	A4	4	2	5	3	0	5	9	2/24/81	Bell et al.	365	185.22		
TP	A5	4	2	7	2	8	3	0	6/9/81	Moench	365	45		
TP	A6	4	2	7	9	0	2	4	7/14/81	Schrenk	365	184		
TP	A7	4	2	8	7	5	7	0	9/1/81	Stark	365	104		
TP	A8	4	3	9	3	4	7	5	7/12/83	Kitagawa et al.	365	185.21		
TP	A9	4	4	1	5	9	9	2	11/15/83	Adlhoch	365	207		
TP	A10	4	4	6	0	9	8	2	7/17/84	Gee et al.	365	185.22		
TP	A11	4	4	9	5	6	0	2	1/22/85	Sheppard	365	203		
§ FOREIGN PATENT DOCUMENTS														
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TP	B1	GB	2	0	6	1	6	5	1	5/1981	United Kingdom	—	—	
TP	B2	GB	2	0	2	9	1	4	5	3/1980	United Kingdom	—	—	
TP	B3	JP6	6	2	2	5	7	6	9	10/1988	Japan	—	—	Abstract
TP	B4	JP	5	9	3	1	1	5	8	2/1984	Japan	—	—	Abstract
TP	B5	DE	3	6	3	7	6	8	2	5/1987	Germany	—	—	Abstract
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)														
TP	C1	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells", IEEE Journal of Solid-State Circuits, vol. sc-22, No. 3, June 1987, pp. 460-463.												
TP	C2	Torelli et al., "An Improved Method for Programming a Word-Erasable EEPROM", Alta Frequenza, Vol. 52, Nov. - Dec. 1983, no. 6, pp. 487-494.												
TP	C3	Stark, "Two Bits Per Cell ROM", Digest of Papers of Spring COMPCONS 81, Feb. 23-26, VLSI LABORATORY, pp. 209-212.												
EXAMINER <div style="text-align: center; font-size: 1.2em;">Trong Phan</div>										DATE CONSIDERED <div style="text-align: center; font-size: 1.2em;">10/5/2000</div>				
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TP	A12	4	5	8	6	1	6	3		4/29/86	Koike	365	104	
TP	A13	4	6	1	2	6	2	9		9/16/86	Harari	365	185.08	
TP	A14	4	7	1	8	0	4	1		1/5/88	Baglee et al.	365	185.22	
TP	A15	4	7	3	3	3	9	4		3/22/88	Giebel	365	201	
TP	A16	4	7	5	2	9	2	9		6/21/88	Kantz et al.	365	201	
TP	A17	4	7	6	3	3	0	5		8/9/88	Kuo	365	185.22	
TP	A18	4	7	7	9	2	7	2		10/18/88	Kohda et al.	365	185.09	
TP	A19	4	7	9	9	1	9	5		1/17/89	Iwahashi et al.	365	185.21	
TP	A20	4	8	0	7	1	8	8		2/21/89	Casagrande	365	185.05	
TP	A21	4	8	0	9	2	3	1		2/28/89	Shannon et al.	365	201	
TP	A22	4	8	1	1	2	9	4		3/7/89	Kobayashi et al.	365	185.22	

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TP	B6	DE	3	8	3	1	5	3	8	3/1989	Germany	—	—	Abstract
TP	B7	JP	62	1	8	8	1	0	0	8/1987	Japan	—	—	Abstract
TP	B8	JP	0	1	2	3	8	7	8	5/1989	Japan	—	—	Abstract
TP	B9	JP	0	1	4	6	9	4	9	10/1989	Japan	—	—	Abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

TP	C4	Furuyama et al, "An Experimental 2-BIT/CELL Storage Dram for Macro Cell or Memory-on-Logic Application", IEEE Custom Integrated Circuits Conference, May 1988, pp. 4.4.1 - 4.4.4												
TP	C5	Krick, "Three-State MNOS FET Memory Array", IBM Technical Disclosure Bulletin, Vol. 18, No. 12, May 1976, pp. 4192-4193.												
TP	C6	Alberts et al, "Multi-Bit Storage Fet Earom Cell" IBM Technical Disclosure Bulletin," Vol. 24, No. 7A, Dec 1981, pp. 3311-3314, 4193.												

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TP	A23	4	8	4	7	8	0	8		7/11/89	Kobatake	365	104	
TP	A24	4	8	7	0	6	1	8		9/26/89	Iwashita	365	185.18	
TP	A25	4	9	4	3	9	6	2		7/24/90	Imamiya et al.	365	230.08	
TP	A26	4	9	5	6	8	1	6		9/11/90	Atsumi et al.	365	185.22	
TP	A27	4	9	9	9	8	1	3		3/12/91	Ohtsuka et al.	365	185.18	
TP	A28	5	0	0	3	5	1	0		3/26/91	Kamisaki	365	189.01	
TP	A29	5	0	5	3	9	9	0		10/1/91	Kreifels et al.	365	185.02	
TP	A30	5	0	9	5	3	4	4		3/10/92	Harari	257	328	
TP	A31	5	1	3	6	0	2	1		11/10/92	Mehrotra et al.	530	350	
TP	A32	5	2	9	7	1	4	8		3/22/94	Harari et al.	365	185.33	
TP	A33	5	3	5	7	4	6	2		10/18/94	Tanaka et al.	365	185.22	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

TP	C7	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-LEVELS/CELL Storage" IEEE Journal of Solid-State Circuits, Vol. 23, Feb 1988, No. 1, pp. 27-33.
TP	C8	Masuoka et al., "A 256-KBIT Flash EEPROM using Triple-Polysilicon Technology" IEEE Journal of Solid-State Circuits, vol.SC-22, no.4, pp 548-552, New York, US, August 1987
TP	C9	Berenga et al., "E2-PROM TV Synthesizer", 1978 IEEE International Solid-State Circuits Conference: ISCCC 78," February 17, 1978, pp.196-197.

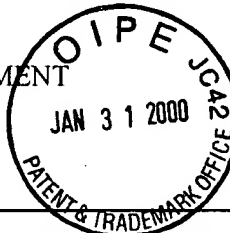
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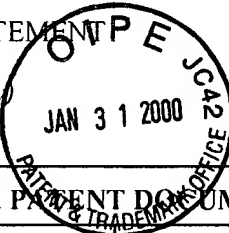
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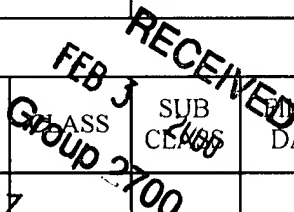
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U. S. PATENT DOCUMENTS													
*EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUB CLASS	FILING DATE
TP	A34	5	3	6	1	2	2	7	11/1/94	Tanaka et al.	365	185.22	
TP	A35	5	6	0	2	9	8	7	2/11/97	Harari et al.	365	200	
TP	A36	4	9	5	9	8	1	2	9/25/90	Momodomi et al.	365	185.17	
TP	A37	4	9	3	9	6	9	0	7/3/90	Momodomi et al.	365	185.17	
TP	A38	4	9	9	6	6	6	9	2/26/91	Endoh et al.	365	185.17	
TP	A39	5	1	6	3	0	2	1	11/10/1992	Mehrotra et al.	365	185.03	
TP	A40	5	1	7	2	3	3	8	12/5/1992	Mehrotra et al.	365	185.03	
TP B1	A41	5	1	7	2	3	3	8	7/9/1997	Mehrotra et al. (Reexamination)	365	185.03	
TP	A42	5	6	5	7	2	7	0	8/12/1997	Ohuchi et al.	365	185.22	
TP	A43	5	7	9	3	6	9	6	8/11/1998	Tanaka et al.	365	230.06	
TP	A44	5	8	3	1	9	0	3	11/03/1998	Ohuchi et al.	365	185.22	
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TP	C10	Kynett et al., "An In-System Reprogrammable 32K X 8 CMOS Flash Memory", IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, Log Number 8822443, October 1988, pp. 1157-1163.											
TP	C11	Klingman, "Microprocessor Systems Design" Prentice-Hall Inc., pp. 30-31, 1977.											
TP	C12	SGS-Ates, "Excerpts From a 1983 Data Book" SGS-Ates Group, 45 pp., Nov. 1983.											
TP	C13	Torelli et al, "Non-Volatile Station Memory and Remots-Control Receiver and Memory-Display Driver" IEEE Transactions on COnsumer Electronics, vol. CE-29, no. 3, pp. 103-13, August 1983.											
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TP	A45 4 6 7 7 5 9 0	6/30/1987	Arakawa	365/185.17							
TP	A46 4 9 8 0 8 6 1	12/25/1990	Herd et al.	365	185.17						
TP	A47 4 4 7 5 1 9 4	10/1984	LaVallee et al.	365	200						



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OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent pages, Etc.)</i>	
TP	C14 Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver in a Single Chip" IEEE Digest of Technical Papers, Cat. No. 83CH1872-1, 2 pp., June 8, 1983.
TP	C15 Caironi et al., "A TV Frequency Synthesis System With A Single Chip Microprocessor Interface Including Non Volatile Memory" IEEE Transactions on Consumer Electronics, vol. CE-28, no. 3, pp. 363-71, August 1982
TP	C16 Torelli, "An LSI Technology Fully Compatible EAROM Cell":S-ATES Componenti Elettronici SpA, no. 6, vol. LI, 7 pp., 1982.
TP	C17 Torelli et al., "PLL2K-PLL Frequency Synthesizer for 30 Programs" SGS-ATES, Technical Note #152, pp. 1-16, 1982.

EXAMINER <div style="text-align: center; font-family: cursive; font-size: 1.2em;">Trong Phan</div>	DATE CONSIDERED <div style="text-align: center; font-family: cursive; font-size: 1.2em;">10/5/2000</div>
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